Design of Reliable Body Channel Communication Transceiver with Spread Spectrum Clock Generator and PNR Generator

S.Vijayalakshmi
Ph.D. Research Scholar, Department of ECE,
Adhiparasakthi Engineering College,
Melmaruvathur, Chennai, Tamil Nadu, India-603 319.
sankarviji7@gmail.com

V.Nagarajan
Professor, Department of ECE,
Adhiparasakthi Engineering College,
Melmaruvathur, Chennai, Tamil Nadu, India-603 319
nagarajanece31@gmail.com

Abstract—In this work, the communication of a channel in the human body has a characteristic (time-domain) which can be measured at various distances in transmission and various frequencies of a signal by the printed circuit board-an analog frontend board (PCB-AFE) support. Besides, for the wideband signal of Body Channel Communication (BCC), a human body skin acts within a range of 1 Mb/s to 40 Mb/s as the transmission medium. This communication is more stable and attenuating low power while comparing with all another transmission medium in wireless. Moreover, due to the motion of a human body, this communication doesn't get affected. Though, the body antenna gives effects in the communication of a channel of the human body by occurs some interference. The Manchester data acts as encoder and decoder in transmitter and receiver parts respectively, in an AFE-PCB the Manchester encoder data is amplified after receiving the data from end to end channel of a human body. The data quality is improved by 7X sampler in clock data recovery (CDR) circuit. Therefore, the proposed design of reliable BCC Transceiver with SSCG and PNR Generator is processed in XilinxISE14.5, ModelSim Simulator 6.5a (Quartus II 8.1), and Micro wind software tools. It is also implemented in a XilinxXC9572XL kit. The power consumption and delay is reduced up to 90%, speed is increased up to 50% and leakage current is reduced up to 80% in the transmitter part.

Index Terms—Analog Front End (AFE), Body Channel Communication (BCC), Clock Data Recovery (CDR), Printed Circuit Board (PCB), Reconfigurable Frequency Synthesizer (RCFS) and Variable Cymometer (VC).

I. INTRODUCTION

In progress eras, a Body-Channel Communication (BCC) is one of the greatest inspiring motivations to the canvassers. The canvasser becomes new involved in body communication is for the reason that the process is done in low-power. A BCC and BAN-Body Area Network are different. A BCC is formally well-defined as, "An operations boosted for low in power customary of communication and operates in/on/over the body of a human for range portion of uses such as personal entertainment, medical, consumer electronics etc." by an IEEE standard 802.15. The wearable electronic approaches types like wrist-type computers, earphones, a head-mounted display and video eyeglasses are used in the interior of a human-body to preserve the normal connection and also for furthermore communication. In normal type, the BCC analyses this association and therefore it values the standard communication for a human body. This association type is much nearer to the body of a human, via entry devices it can interconnect with external work [1-5].

At frequencies MHz, the BCC can work for the cause with the large couplings needy that through the transceiver a lot of signals can transmit which coupled to the capacitive ground and a body of a human. The power consumption maximum value is due to the capacitance of low impedance. So, reduction of power is one of the greatest opportunities ended by via a low-impedance coupling capacitance. This communication scheme type has numerous applications like monitoring the human being with the cardiac system and also evaluating the blood pressure etc. Most recent eons, the handshake business card, and code unlocks for door etc. are successfully used as improved applications with lots of BCC system types. This established communication is since of coupling the human body with capacitive and an electrical field is followed by the data transmission. In current days, the body of a human is getting importance because of the natural connection with it, in the human setting of communication-centric [6-9].

The magnetic field coupling is also said to be as the Near Field Communication (NFC) which is established on the Radio Frequency Identification (RFID) Technology. To moderate the application scope, the RFID technology is used to limit the definition of NFC. In 1995, the BCC is in starting point in the field of biomedical; it becomes valued applications by recovering its position in present existences.

The KAIST and Philips research groups mostly establish the BCC for biomedical application to check the health condition of the patient from the faraway location. There are two portions in a transceiver of BCC: The baseband digital is the main and the

IRJECE

This is an open access article under the CC BY-SA 4.0 license (https://creativecommons.org/licenses/by-sa/4.0/)

next is an AFE-Analog Front End. As a BCC frequency, the body of a human organizes. The consideration of simple communication standard is as a lesser field of electric that permits over the body of a human to transmit the frequency signal about to the devices, so they can be in contact to a body of a human directly [10-11]

The main idea of the total system is to consume a power. To maintain the better consumption in power, the standard group of IEEE 802.15.6 is used to plan for BCC. For the consumption in power, the BCC allows to transmit the data rate. An electrical coupling is also named as the aforementioned communication for far field which produces BCC as sustain for maintaining the rate of data and consume the power. On a regular base, some maintenance should be desired by human to approve that the health condition of body is good. Thus to check the parameters physiologically and continuously, the BCC is established to deal to withstand the body of a human. Consequently, this monitoring type produces records through an electronic equipment in the medical field which is used for physicians to work simple in the health-care engineering.

Though aspects affected by many energy consumptions in WBANs (for, e.g., unit processing and the hardware sensors design, in count to the processing in data and techniques /algorithms, actuators), definitely an era and also the major supporters for communication develops extra to the consumption of an energy quantity by the society[12].

This frame work of paper is exposed as below. Sector II has basic process explanation in BCC Transceiver. Sector III explains about the SSCG-PNR method. Sector IV talk over about the outcome. At last, Sector V accomplishes by the paper.

II. BCC Transceiver Simple Method

The scheme of BCC transceiver is to apprehend its characteristics in a channel. It covers a PCB with AFE, receiver, and transmitter. An AFE PCB consists of a variable gain amplifier and a Schmitt trigger. The design of BCC transceiver is as shown in Fig. 1. The system operation depiction is mentioned as below: An encoded input in the form of Manchester data is given to the transmitter which transmits the data to the human body which is interconnected with the buffer driver. The body of the human exhibits AFE_IN signal like shark fin signal to an AFE-PCB located at the receiver section. The resulted AFE_IN signal is converted to digital waveform with VGA amplification at once the Schmitt trigger process got completed. Previously the clock signal gets as output and the Manchester data is recovered by the receiver of BCC.

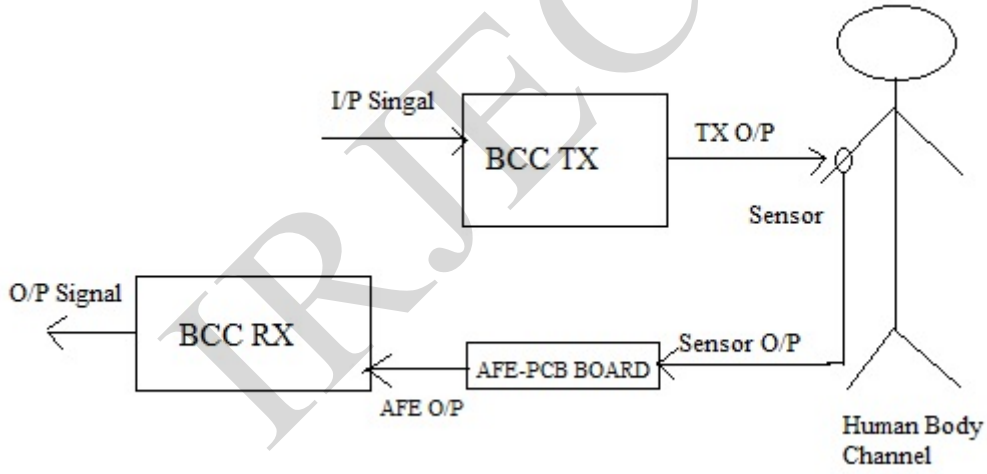


Fig.1. BCC Transceiver Design

III. SSCG-PNR Method

Refer to Fig. 2: The BCC transmitter which is shown here comprises of a preface generator, a Manchester encoder and Spread Spectrum Clock generator (SSCG) with the control of bit stuffing. In order to reduce the electromagnetic interference (EMI), the transmitter needs to be triggered. So at the part of transmitter, the spread spectrum clock signal is generated by the SSCG circuit which is built in the transmitter. A checking circuit consists of XOR gate in Linear Feedback Shift Register of the transmitter.

Hence, through the channel of a human body, the data of 1000 bytes are used to transmit continuously. After first packet transmission, the second packet is transmitted to the human body and it is so on continued. In the receiver of WBS BCC, the PCB is provided with the all-digital clock and data recovery (ADCDR) circuit. The wideband pulse signals from the human body channel are received by an AFE PCB which is then improve the signals to digital waveforms.

IRJECE

This is an open access article under the CC BY-SA 4.0 license (https://creativecommons.org/licenses/by-sa/4.0/)

Here the registers are helpful to measure the bit error rate by producing the random pattern sequences. Two multiplexers are used in the normal mode to select the clock input externally or data input externally. With the help of buffer driver, the TX_DATA gets encoded by the Manchester encoder to transmit data through the body channel of human.

In the part of receiver, it is difficult to recover the data by increasing the less data transitions happens due to accumulation of jitter in the AFE-PCB and the distortion of duty-cycle. Because of this, the data transitions are more sufficient after Manchester encoding to create the stuffier bit in the transmitter.

The maximum values of continuous Identical Digits (CID) are 5 bits after the control of bit stuffing. To go along with the start frame delimiter (SFD) consisting of four bits and to get a synchronization packet, the sixteen bits of preamble are transmitted through a channel of human body at first.

To get the signal of clock and data, the circuit of CDR 7X sampler recovers the signals of AFE output finally. The CDR circuit mainly consists of a Manchester decoder, a variable cymometer, a reconfigurable frequency synthesizer (RCFS), a vote integrator, a LFSR checking circuit and a 7x sampler.

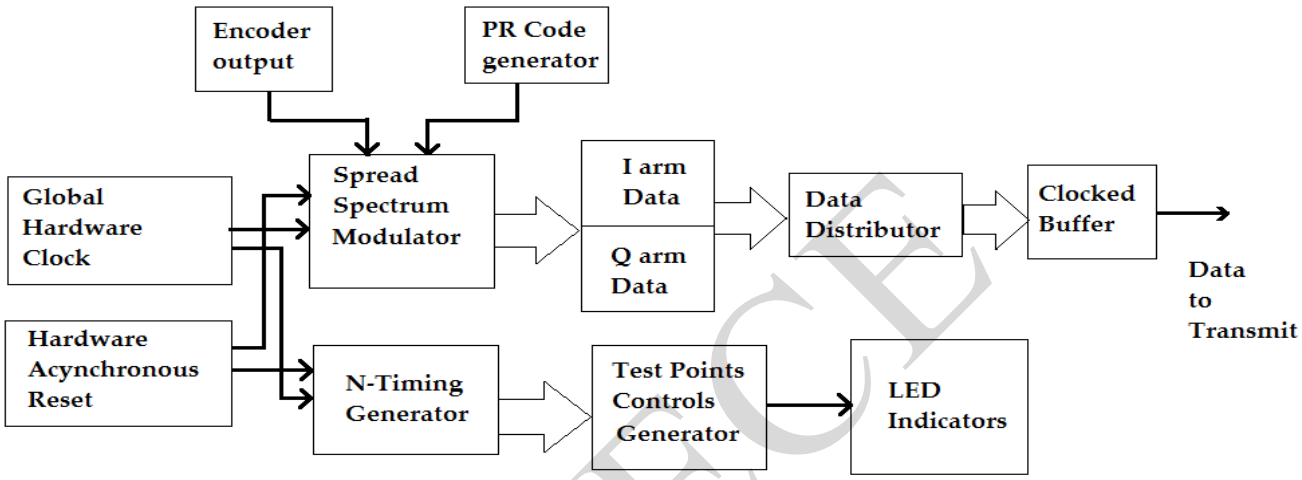


Fig. 2. BCC Transmitter Part

A. *Spread Spectrum Clock Generator*

Spread Spectrum Clock Generator (SSCG) is a frequency modulation (FM) method which is used to reduce EMI radiation generated by repetitive digital signals mainly through clocks. The EM energy radiated by clock has fundamental frequency and its harmonics also. Over a small frequency bandwidth, this energy is distributed by Spread Spectrum. Also over the spectrum, the peak value of radiated energy is decreased. By modulating the clock signal around or below the center of its reference frequency by a certain percentage, this technique is achieved. This one also determines the bandwidth of energy distribution. When SSON pin is set to low, the SSCG function is enabled, resulting in a center spread or spread bandwidth as the amount selected by SSSEL.

i. *Spread Spectrum Clocks:*

To spread the spectrum of a digital clock signal, two fundamental different ways are there. In suppressed carrier clocking or clock scrambling, via an XOR gate, the clock signal is mixed directly with a modulation signal. The most widespread practice for clock signal conditioning consists of the clock frequency modulation with a waveform to spread its energy, which is shown in Fig. 3.

According to theory, the jitter does not get introduced by suppressed carrier clocking. The fundamental attenuation is little greater than 10dB. Even though there are main drawbacks to clock scrambling. During the transitions of modulating signals, there is a loss of transition on the suppressed clock. This accounts to lost computation time of a digital system. To preclude this problem, at the various ends of the clock distribution network, the scrambled signal can be demodulated but this process leads to addition of demodulation circuitry. This involves that only the clock distribution network signal has suppressed EMI, whereas the signal in the remaining of the chip release radiation at the clock frequencies and harmonics.

The attenuation can be greater once the greater the deviation, and slower the frequency of modulating signal.

Obviously, the digital systems timing constraints being clocked will offer a practical limit to the tolerable amount of deviation.

IRJECE

This is an open access article under the CC BY-SA 4.0 license (https://creativecommons.org/licenses/by-sa/4.0/)

$$A_{dB} = 10\log_{10}\left(\frac{\delta_{SSC} \cdot n \cdot f_o}{f_{MOD}}\right)$$

There is basically two different ways of obtaining a spread spectrum clock signal at the architecture level. To directly modulate the clock's frequency is the first method. In general, input voltage of a Voltage Controlled Oscillator (VCO) is controlled by a modulation waveform. PLL based SSCG is the industry wide accepted solution for EMI reduction. Several chips are provided for the PCB designer along with patented modulation profile which presents the optimal flatness to the spread spectrum clock. The triangular modulation profile is a simpler technique which reduces efficiency and also simplifies the circuitry involved. A number of peripheral blocks including a phase-frequency detector (PFD) with charge pump output and a VCO are added to one of these techniques. The main advantages of SSCG are high speed operation, an arbitrary spreading sequence and fitting to the entire design in one FPGA.

ii. PNR Generators:

Pseudorandom Binary Sequence (PRBS) generator shown in Fig. 4 produces spreading codes. PRBS is a sequence of random 1's and 0's that repeats at definite intervals. PRBS is generated by shift registers with XOR feedback from the built in hardware. Length of shift register chain and feedback taps decides the length of PRBS. The maximum sequence length = 2n -1 states prior to repeating, where "n" is equal to the length of shift register. In a pseudorandom scrambler and descrambler as well as in a direct-sequence spread-spectrum system, a pseudo noise sequence can be used. This signal is used to hold and release the base band input signals which are used to come from the encoder part of BCC TX or from the memory. For applications such as gaming and generating encryption/decryption keys in which unpredictability of binary numbers is the most desirable feature, PRNGs are not suitable. The features of PRNGs make these generators suitable for applications such as digital communication, modeling, simulation and fault grading.

In the generation of spread spectrum clock signal, PRC generation is one of the important aspects concerned. The raw data signals are nothing but the baseband signals generated for the purpose of efficient spectral generation. In this proposed work, we have implemented a Dynamically Variable PRC Loader (DVPRC-Loader) to increase the encryption stronger for which we dynamically change the loading value with the help of selected frame of clock duration. The initial value of the PRC shifter is updated by Dynamic PRC coder so that only a unique detector can predict the value. PR Codes are generated at regular intervals of time with respect to clock in normal course of operation. Hence at certain stage, the random baseband values become predictable. However the DVPR Coder generates a highly secured random code which cannot be predicted by a normal decryptor as proposed in this design. The information used for communication is high resolution one in case of body channel communication. However the low power test values can be further related to network creation on BCC. Hence the SSCG is designed in such a way that it will be able to generate unique signals for efficient transmission. In a spreaded sequence of digital data, spread spectrum signals are the modulated signals.

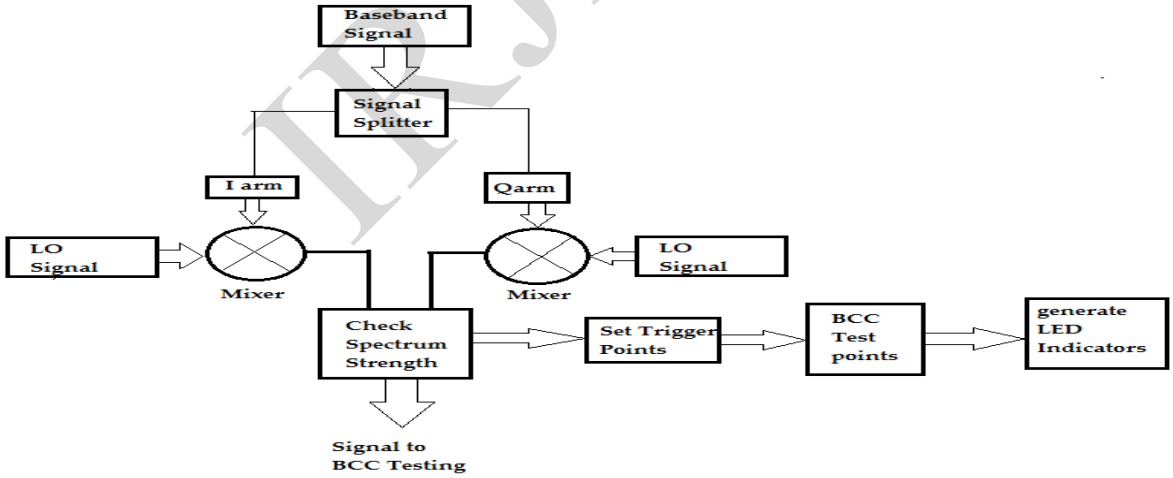
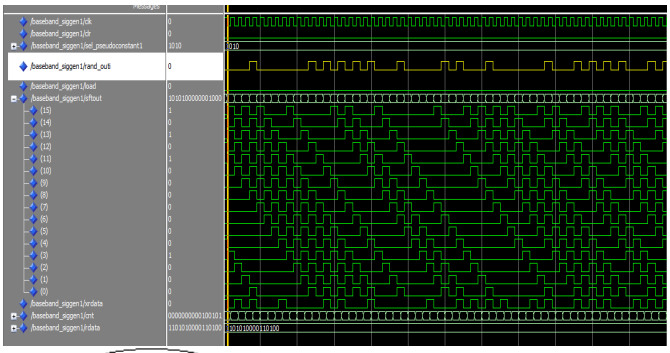


Fig. 3. Spread Spectrum Clock Generator

IRJECE

This is an open access article under the CC BY-SA 4.0 license (https://creativecommons.org/licenses/by-sa/4.0/)



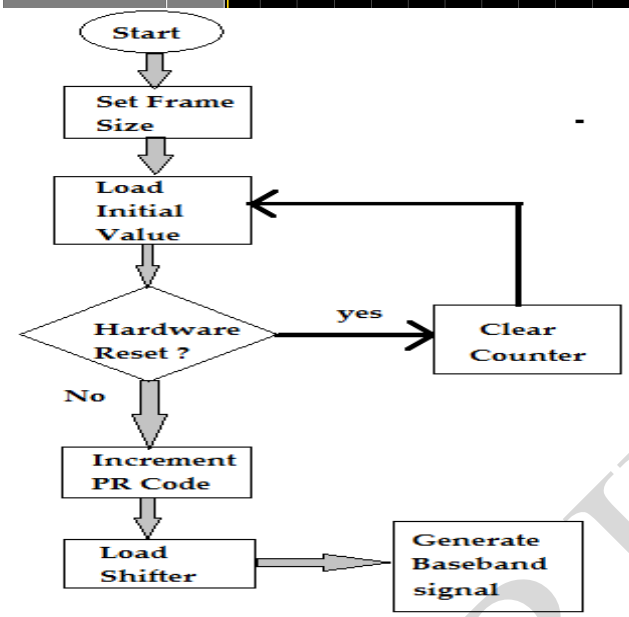


Fig. 4. PNR Generation Flow chart

The spreader signal shall be applicable for less channel interference of signals and for selective frequency in body channel communication due to the advantage of SSCG. SSCG signals generate a unique channel frequency which is useful to access the exact device even though when a sweep of input communication is held. To make the signal components separately, baseband signals are spread into IARM, QARM. To modulate the frequency and to split up into unique channel frequency, the baseband mixer is used.

The proposed BCC receiver's fundamental function was explained above. In order to achieve low-power and high speed processes in receiver part, the RCFS synthesis code and VC device were used.

IV. Simulation Results

i) PNR Generation output

The output Fig. 5 shows the PRN input generation through auto updating sequence. Rand_outI is the outpuit of the module. 16 Bit input data is used to run the generator. Rdata is the input data which we load initially. Set_pseudoconstant1 is the selection bit for initial data which is loaded.

Fig. 5. PNR Generation output

ii) LED Test point for detecting the analyzing the output values

This output Fig.6 generates a square wave at every 30 Second which is connected to a LED flag to enable the test point. Every 30 second you can read and verify the BCC vectors for testing purpose. Test points are mandatory during testing phase of the proposed work. Like 30 sec pulse, we also given a 60 sec, 90 sec and 150 sec pulse. Depends on the SSCG signal generated these pulse selection will be changed.

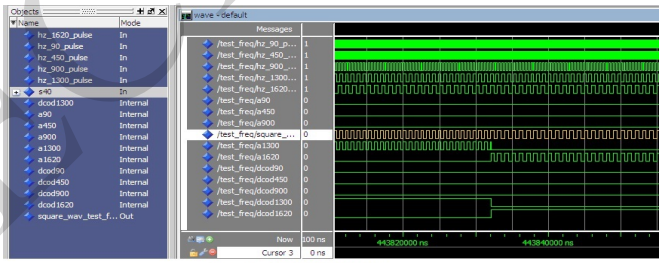
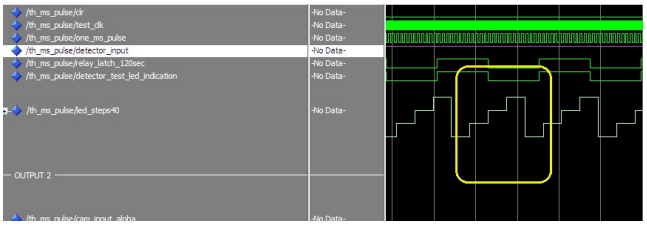


Fig. 6. Square wave test output for LED TEST 30 s

iii) Dimming LEDS outputs

This o/p is useful to check the changing phase of the SSCG from one frequency to another fixed frequency spectrum. The stepped LED o/p is shown below which is nothing but the changing or Resilient phase of the spectral change which is shown in Fig.7 and Fig.8



IRJECE

This is an open access article under the CC BY-SA 4.0 license (https://creativecommons.org/licenses/by-sa/4.0/)

Fig. 7. Spectral change @ 120 seconds, for every 40 sec LED Light get dimmer to stronger

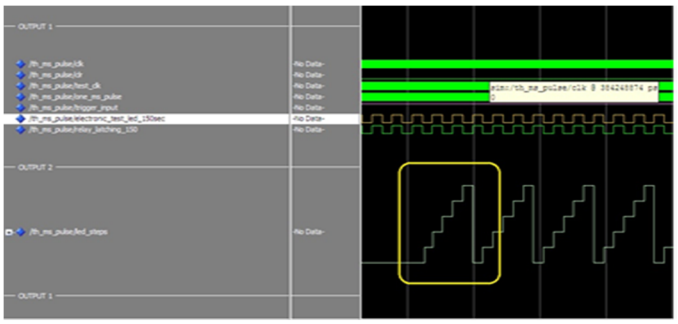


Fig. 8. Spectral change @ 150 seconds

i) Initial Trigger

Trigger input is used to initiate all the parameters for few seconds so that the spectral constants are getting intiated which is shown in Fig. 9.

Fig. 9. Asynchronous trigger pulse at the Input

The integration first output carries all LED types are given with 30sec, 40sec, 60sec 120sec and 150sec which is shown in the Fig.10.

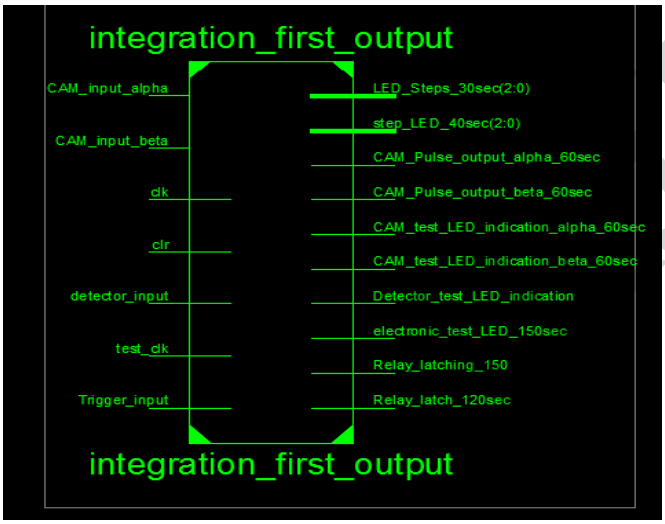


Fig. 10. Integration first output

Here, the number of slices registers, 4 input LUTs, occupied slices, bonded IOBs, BUFGMUXs and average non-clock nets fan-out are used with the values of 185, 202, 191, 19, 2 and 2.30 respectively as shown in Fig. 11. The overall utilization is 0.09% only.

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	185	9,312	1%	
Number of 4 input LUTs	202	9,312	2%	
Number of occupied Slices	191	4,656	4%	
Number of Slices containing only related logic	191	191	100%	
Number of Slices containing unrelated logic	0	191	0%	
Total Number of 4 input LUTs	341	9,312	3%	
Number used as logic	202			
Number used as a route-thru	139			
Number of bonded IOBs	19	232	8%	
Number of BUFGMUXs	2	24	8%	
Average Fanout of Non-Clock Nets	2.30			

Fig. 11. Integration first output

Fig. 12 shows the power calculation where the clocks, logic, signals, Ios, leakage power utilization is calculated. The overall power consumption is 0.081W.

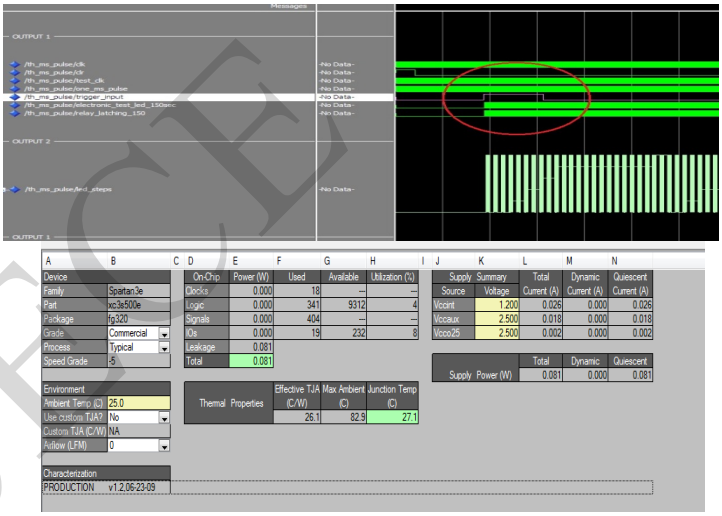


Fig. 12. Integration first output

The output in Fig. 13 has shown the DS-SS Signal and Multiplier output sequence without correlation noise.

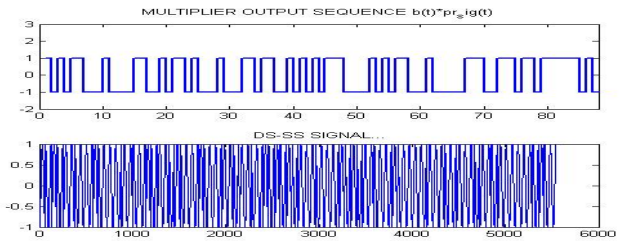


Fig. 13. Integration first output

This is an open access article under the CC BY-SA 4.0 license (https://creativecommons.org/licenses/by-sa/4.0/)

Table I shows the values of all parameters such as the power consumption in a XilinxXC9572XL board is 0.081W. Here it has 0.09% utilization in device for 1Mb/s to 40Mb/s.

V. Conclusion

At different times, the Body-Channel Communication (BCC) is accessible in various transceivers. As the received signal carries all data/information, we have to give more importance to the performance of jitter and glitch. In order to maintain the high gain, there may be signal attenuation because of the human body motion. As we could find, power consumption plays a vital role in a communication. In this paper, the design of reliable BCC Transceiver with SSCG and PNR generator are simulated in Xilinx ISE 4.5, ModelSim Simulator 6.5a (Quartus II 8.1), MatLab tool and implemented in XilinxXC9572XL kit. In this proposed transmitter, all the above basic requirements are preserved. The analysis resulted through this paper is used to provide moral conditions to enhance performance of the transmitter.

Acknowledgment

The authors wish to thank the Adhiparasakthi Institution for supporting us to complete the work successfully.

References

[1] Namjun Cho., et al. (2009). A 60kb/s - 10Mb/s adaptive frequency hopping transceiver for interference-resilient body channel communication. *IEEE Journal of Solid-State Circuits*. 44(3), 708-717.

[2] Juha Petäjäjärvi., et al. (2016). On the human body communications: wake-up receiver design and channel Characterization *EURASIP Journal on Wireless Communications and Networking*. doi:10.1186/s13638-016-0674-5.

[3] IEEE Computer Society. (2012). IEEE standard for local and metropolitan area networks: part 15.6: wireless body area networks. *IEEE Standards Association*.

[4] Mitsuru Shinagawa., et al. (2004). A near-field-sensing transceiver for intrabody communication based on the electrooptic effect. *IEEE Transactions on Instrumentation and Measurement*. 53(6), 1533-1538.

[5] T. G. Zimmerman. (1996) Personal area network: Near-field intrabody communication. *IBM Systems Journal*. 35(3&4), 609-617.

[6] Nie Zedong., et al. (2014). An investigation on dynamic human body communication channel characteristics at 45 MHz in different surrounding environments. *IEEE Antennas and Wireless Propagation Letters*. 13, 309-312.

[7] Namjun Cho., et al. (2007). The human body characteristics as a signal transmission medium for intrabody communication. *IEEE Transactions on Microwave Theory and Techniques*. 55(5), 1080-1086.

[8] Xingqiang Peng., et al. (2017). A 2.4-GHz ZigBee Transmitter Using a Function-Reuse Class-F DCO-PA and an ADPLL Achieving 22.6% (14.5%) System Efficiency at 6-dBm (0-dBm) Pout. *IEEE Journal of Solid-State Circuits*. 52(6).

[9] Sandro Cadeddu., et al. (2017). A Time-to-Digital Converter Based on a Digitally Controlled Oscillator. *IEEE Transactions on Nuclear Science*, 64(8), 2441.

[10] Marijn Verbeke., et al. (2017). A 1.8-pJ/b, 12.5–25-Gb/s Wide Range All-Digital Clock and Data Recovery Circuit. *IEEE Journal of Solid-State Circuits*. doi:10.1109/JSSC.2017.2755690

[11] Lei Wang., et al. (2017). An ADPLL based PSK Receiver for VHBR 13.56MHz Contactless Smartcards and NFC Applications. *IEEE Transactions on Circuits and Systems II*. doi:10.1109/TCSII.2017.2763986.

[12] Safeen Huda., et al. (2017). Leveraging Unused Resources for Energy Optimization of FPGA Interconnect. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*. doi:10.1109/TVLSI.2017.2691409.

TABLE I
Comparison of Parameter Values

Parameter	Proposed Values	Existing Values
Process	Xilinx ISE 14.5 Process	CMOS 90nm Process
Operating Range	1Mb/s to 40Mb/s	1Mb/s to 40Mb/s
Supply	1V	1V
Power Consumption	XilinxXC9572XL:0.081W	1.21mW
Device Utilization	0.09%	0.144mm^2

IRJECE

This is an open access article under the CC BY-SA 4.0 license (https://creativecommons.org/licenses/by-sa/4.0/)